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REMARKS

Applicant respectfully requests the Examiner's reconsideration of the present application as amended.

Claims 1-9, and 26-36 are pending in the present application.

Claims 1-9, and 26-36 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,396,435 ("Ginetti").

Claims 1, 8, 26, 33, 35, and 36 have been amended.

Support for amended claims 1, 26, and 35 is found on page 14, line 21 though page 15, line 15, and Figures 4 and 7. Support for amended claims 8, 33, and 36 is found on page 16, line 20 through page 21, line 4, and Figures 10-13. No new matter has been added.

Claims 1-9, and 26-36 are rejected under 35 U.S.C. §102(b) as being unpatentable over Ginetti. More specifically, the Office Action mailed 1/18/2007 states in part that

> As to claims 1, 26 and 35 Arnold Ginetti teaches a method for designing a system on a target device utilizing field programmable gate arrays (FPGA), comprising: identifying a group of components associated with a critical signal in the system (see fig 3a, 3b, col 3 line 40 to col 4 line 15, and abstraction); creating a first copy and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal (see fig 3a-3c, fig 4 and fig 6a-6c col 3 line 45 to col 8 line 42); and configuring the system to select an output of one of the first coopy and the second copy in response to the critical signal (see fig 3a-3c, fig 4, fig 6a-6c col 7 line 4 to col 8 line 68).

(1/18/2007 Office Action, p. 2).

It is submitted that Ginetti does not render claims 1-9, and 26-36 unpatentable under 35 U.S.C. §102(b).

Ginetti includes a disclosure of a computer aided design system that automatically modifies a specified circuit netlist to reduce signal delays on critical signal paths. A critical signal path that does not meet specified timing constraints is identified by computing signal slack values for each node, where negative slack values indicate a failure to meeting timing requirements. Critical gates along the critical signal path that are candidates for duplication are identified by determining which critical gates have a fanout greater than one and can be represented by library cells compatible with the next circuit tree along the critical signal path. One such gate is selected and duplicated, with one copy of the duplicated output gate being used to generate only the signal on the critical signal path and the other copy of the duplicated output gate being used to drive all other fanouts of the selected gate. This generates a modified circuit netlist. Then slack values for the modified circuit netlist are compared with those of the previous version of the circuit netlist. If the slack values of circuit on the critical path have been improved, the modified circuit netlist is adopted as the current circuit netlist. If any node in the adopted circuit netlist has a negative slack value, the circuit netlist modification procedure is repeated until either no node has a negative slack, or the process is unable to further improve the slack values of the circuit netlist (Ginetti Abstract).

It is submitted that Ginetti does not teach or suggest identifying a group of components associated with a critical signal in the system, creating a first copy and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state, and configuring the system to utilize a selector circuit on a target device to select an output of one of the first copy and the second copy in response to the critical signal.

On the contrary, Ginetti illustrates a critical signal path in Figure 3B (see Ginetti col. 6, lines 50-52). Gate H in the circuit of Figure 3B is duplicated, producing a second gate H* illustrated in Figure 6A (see Ginetti col.8, lines 16-19). The outputs of gate H and gate H*, however, are always utilized by the logic in the circuit. The output of gate H is always inputted to Tree B and the output of gate H* is inputted to logic in Tree A (see Ginetti Figures 6A, 6B, and 6C). Ginetti does not teach or suggest utilizing a selector circuit to select an output of one of gate H and gate H* in response to a critical signal. Applicants submit that Ginetti does not illustrate any selector circuit in Figures 6A, 6B, or 6C.

In contrast, claim 1 states

> A method for designing a system on a target device utilizing field programmable gate arrays (FPGAs), comprising:
> identifying a group of components associated with a critical signal in the system;
> creating a first copy and a second copy of the group of components where the first copy is driven by a first signal at a first state and the second copy is driven by a second signal at a second state; and
> configuring the system to utilize a selector circuit on the target device to select an output of one of the first copy and the second copy in response to the critical signal.

(Claim 1 as amended) (Emphasis Added).

Claims 26 and 35 similarly include the limitation of utilizing a selector circuit to select an output of one of the first copy and the second copy in response to the critical signal. Given that claims 2-9, 27-34, and 36 depend from claims 1, 26, and 34, it is likewise submitted that claims 2-9, 27-34, and 36 are also patentable under 35 U.S.C. §102(b) over Ginetti.

Applicants further submit that Ginetti does not teach or suggest removing unused components from the group of components associated with the critical signal.

The Office Action mailed 1/18/2007 states in part that

> As to claim 6 and 31 Arnold Ginetti teaches further comprising removing unused components from the group of components (see fig 3a-3c col 8 lines 13-55, and background).

(1/18/2007 Office Action, p. 3).

Applicants submit that the critical signal path is illustrated by the bold line in Figure 3B (see Ginetti col. 6, lines 50-52). As shown in Figures 3C, 6A, 6B, and 6C, all of the logic along the critical signal path, as shown originally in Figure 3B, continue to be used and remain on the circuit. The connections to the logic, the positioning of the logic, and the labeling of the logic may be changed, but Ginetti does not illustrate unused logic that is removed.

In contrast, claim 6 states

> The method of Claim 1, further comprising removing unused components from the group of components.

(Claim 6) (Emphasis added).

Claim 31 includes similar limitations.

Applicants further submit that Ginetti does not teach or suggest determining appropriate placement of the first copy and the second copy on the target device using an incremental placement technique to resolve illegalities in placement by moving components not associated with the critical signal to allow the first copy and the second copy to be placed at preferred locations.

The Office Action mailed 1/18/2007 states in part that

> As to claim 8, 33, and 36 Arnold Ginetti teaches further comprising determining appropriate placement of the first copy and the second copy on the target device using an incremental placement technique (see fig 3a-3c, fig 4 and fig 6a-6c col 3 line 45 to col 8 line 42).

(1/18/2007 Office Action, p. 3).

Applicants submit that Ginetti does not provide any disclosure on how to resolve illegalities in placement. Furthermore the text cited by the Office, column 3, line 45 to column 8, line 42, does not appear to make any reference to placement whatsoever.

In contrast, claim 8 states

> The method of Claim 1, further comprising determining appropriate placement of the first copy and the second copy on the target device using an incremental placement technique to resolve illegalities in placement by moving components not associated with the critical signal to allow the first copy and the second copy to be placed at preferred locations.

(Claim 8 as amended) (Emphasis added).

Claims 33 and 36 include similar limitations.

In view of the amendments and arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1-9, and 26-36 should be found to be in condition for allowance.

The Examiner is invited to telephone Applicant's attorney (217-377-2500) to facilitate prosecution of this application.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

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LM. Cho
Lawrence M. Cho
Attorney for Applicant
Registration No. 39,942

P.O. Box 2144
Champaign, IL 61825
(217) 377-2500